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HIGH PERFORMANCE STRAINED CMOS DEVICES

Abstract

A semiconductor device and method of manufacture provide an n-channel field effect transistor (nFET) having a shallow trench isolation with overhangs that overhang Si-SiO_2 interfaces in a direction parallel to the direction of current flow and in a direction transverse to current flow. The device and method also provide a p-channel field effect transistor (pFET) having a shallow trench isolation with an overhang that overhangs Si-SiO_2 interfaces in a direction transverse to current flow. However, the shallow trench isolation for the pFET is devoid of overhangs, in the direction parallel to the direction of current flow.